

A Review on Vedic Multiplier using Reversible Logic Gate

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ABSTRACT: System performance is decided by way of the speed of the multiplier, that is the most important element in the numerous of the application like Microprocessor, Digital signal processing, Quantum Computing etc. Multipliers have large area, long latency and devour huge energy. Hence suitable multiplier structure will increase the performance and overall efficiency of the system. The Vedic multiplier improves the speed of the computation and differing types of reversible gates is use to reduce the power consumption because having capability of reversible calculation that means no data loss take place. Reversible logic has wide application in the developing technologies such as quantum computing, optical computing, Nano-technology and so on. From the survey it is observed that the reversible Vedic multiplier is the pre-eminent in the terms of power, area, delay and quantum cost.

KEYWORDS: Vedic Multiplier, Reversible Logic, UrdhvaTiryakbhayam, Quantum Cost, power, delay.

I. INTRODUCTION

Vedic mathematics is the earliest Indian system of mathematics which in particular offers with Vedic mathematical formulae and their application to numerous branches of mathematics. Vedic mathematics was reconstructed from the earliest Indian scriptures (Vedas) by Sri BharatiKrsnaTirtha after his study on Vedas. He created 16 sutras and 16 upa sutras after vast study in Atharva Veda. The maximum famous amongst those sixteen are NihilamSutram, UrdhvaTiryakbhayam, and Anurupye. It has been found that UrdhvaTiryakbhayam is the maximum efficient among those. The splendor of Vedic mathematics lies in the fact that it decreases otherwise cumbersome looking calculations in traditional mathematics to quite simple ones. This is so because the Vedic sutras are claimed to be primarily based on the natural ethics on which the human thought works. Therefore multiplications in DSP blocks can be performed at faster rate. This is a completely interesting subject and affords a few powerful algorithms which can be applied to numerous branches of engineering [2].

Reversible logic has received excessive attention in the recent years due to their capacity to decrease the power dissipation which is the principle requirement in low power very large scale integration design. It has wide uses in low power complementary metal-oxide semiconductor and optical science, polymer computing, quantum computation and nanotechnology. Irreversible hardware working out results in energy dissipation due to data loss. [18]

Reversible logic is one of the encouraging fields for upcoming low power design technologies. Since one of the necessities of all digital signal processors and other hand held devices is to reduce power dissipation multipliers with excessive speed and lower dissipations are essential. [20]

II. RELATED WORK

In 2011, Prashant .R.Yelekar, Prof. Sujata S. Chiwande [5], introduce reversible logic gates and its applications like Low power CMOS, Quantum computer, Nanotechnology, Optical computing, Design of low power arithmetic and data path for digital signal processing (DSP), Field Programmable Gate Arrays (FPGAs) in CMOS technology for extremely low power, high testability and self-repair.

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 4, April 2016

In 2012, PushpalataVerma [11], designed the 4×4 bit Vedic multiplier is implemented on Spartan xc3s50a-5-tq144 device. The computational path delay of the Vedic multiplier is found to be 13.102 ns. Hence it can be concluded that the performance of the proposed 4×4 bit Vedic multiplier seems to be highly efficient in terms of speed when compared to Conventional multipliers. Reducing the time delay is very essential requirement for many applications and Vedic Multiplication technique is very much suitable for this purpose.

In 2013, Rakshith T.R. and RakshithSaligram [20], proposed the Vedic multiplier using reversible logic in Xilinx 9.2i and MODELSIM with reduced TRLIC and reduced delay.

In 2014, A. ShifanaParween, S. Murugeswari [18], design high speed, area efficient, low power vedic multiplier using reversible logic gate. They compare array multiplier and vedic multiplier using different parameters like no. of gate, number of slices, constant inputs, garbage output, delay, total equivalent gate count, power, quantum cost.

In 2015, Akanksha Kant, Shobha Sharma[19], presented different applications of vedic multiplier like in image compression using discrete cosign transform (DFT) algorithm, in multi-level 2D discrete wavelet transform (DWT) for image processing, in the design of low power asynchronous vedic DSP processor core, in parallel FIR filter, in the design of high speed ASIC design.

III. VEDIC MATHEMATICS

The word “Vedas” which literally means knowledge has derivational meaning as source and boundless store-house of all information. The word Veda as well refers to the sacred earliest Hindu literature that is split into four volumes. Vedas first of all had been surpassed from preceding generation to next generation orally. Later they were transcribed in Sanskrit. [3]

Vedas consist of statistics from many topics such as from religion, astronomy, construction, arithmetic, medication etc. Vedic mathematics isn't only a mathematical wonder however also it's miles logical. That is why Vedic mathematics has such a grade of importance which cannot be criticized. Due to these characteristics, Vedic mathematics has already crossed the boundaries of India and has become a leading topic of research overseas. Vedic mathematics deals with various mathematical operations.

The system of Vedic mathematics is based on 16 Sutras. [9] These Sutras along with their brief meanings are enlisted below alphabetically-

TABLE I
THE 16 VEDIC SUTRAS AND THEIR BRIEF MEANINGS

No.	Sutras	Meanings
1	Shunyamanyat	If one is in ratio, the other is 0.
2	ChalanaKalanabyham	Differences and similarities.
3	EkadhikinaPurvena	By one more than the preceding one.
4	EkanyunenaPurvena	By one less than the preceding one.
5	Gunakasamuchyah	Factors of the sum are equal to the sum of factors.
6	Gunitasamuchyah	The product of sum is equal to sum of the product.
7	NikhilamNavatashcaramamDashatah	All from 9 and last from 10.
8	ParaavartyaYojayet	Transpose and adjust.
9	Puranapurabyham	By the completion or non completion.
10	Sankalanavyavakalanabhyam	By addition and by subtraction.
11	ShesanyankenaCharamena	The remainders by the last digit.
12	ShunyamSaamyaSamuccaye	When the sum is same then sum is 0.
13	Sopaantyadvayamantyam	The ultimate and twice the penultimate.
14	Urdhva-tiryakbhyam	Vertically and crosswise.
15	Vyashτισamanstih	Part and Whole
16	Yaavadunam	Whatever the extent of its deficiency.

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 4, April 2016

IV. REVERSIBLE LOGIC GATE

Reversible circuits are those circuits that don't lose data. Reversible computation in a device can be executed best while the device consists of reversible gates. These circuits can generate specific output vector from every input vector, and vice versa, that is, there is a one-to-one mapping between input and output vectors. Thus, an $N \times N$ reversible gate can be represented as

$$I_v = (I_1, I_2, I_3, I_4, \dots, I_N)$$

$$O_v = (O_1, O_2, O_3, \dots, O_N).$$

Where I_v and O_v represent the input and output vectors respectively.[5]

The following are the vital design constraints for reversible logic circuits. [20]

- Reversible logic gates do not permit fan-outs.
- Reversible logic circuits should have smallest quantum cost.
- The design can be optimized so as to generate smallest number of garbage outputs.
- The reversible logic circuits must use smallest number of constant inputs.
- The reversible logic circuits must use a smallest logic depth or gate levels.

A. Basic Reversible Logic Gates[18]

1) *Feynman gate*: Fig 1 shows a 2×2 Feynman gate. The input vector is $I (P, Q)$ and the output vector is $O (L, M)$. The outputs are defined by $L=P$, $M=P \text{ xor } Q$. Quantum cost of a Feynman gate is 1.

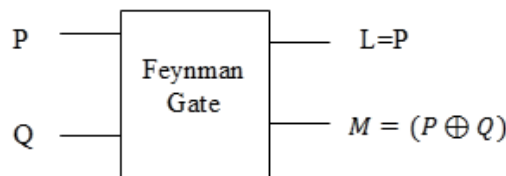


Fig.1 Feynman gate

2) *Peres gate*:Fig 2 shows a 3×3 Peres gate. The input vector is $I (P, Q, R)$ and the output vector is $O (L, M, N)$. The output is defined by $L = P$, $M = P \text{ xor } Q$ and $N=PQ \text{ xor } R$. Quantum cost of a Peres gate is 4. In the proposed design Peres gate is used because of its lowest quantum cost.

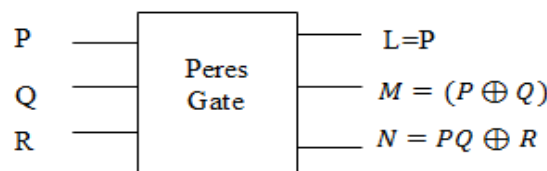


Fig. 2 Peres gate

3) *HNG gate*:Fig 3 shows a HNG Gate. The input vector is $I (P, Q, R, S)$ and the output vector is $O (L, M, N, O)$.The full adder using HNG is obtained with $R= C_{in}$ and $S=0$.

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 4, April 2016

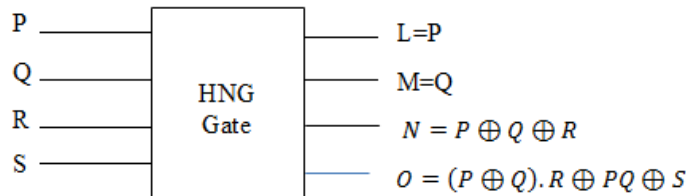


Fig. 3 HNG gate

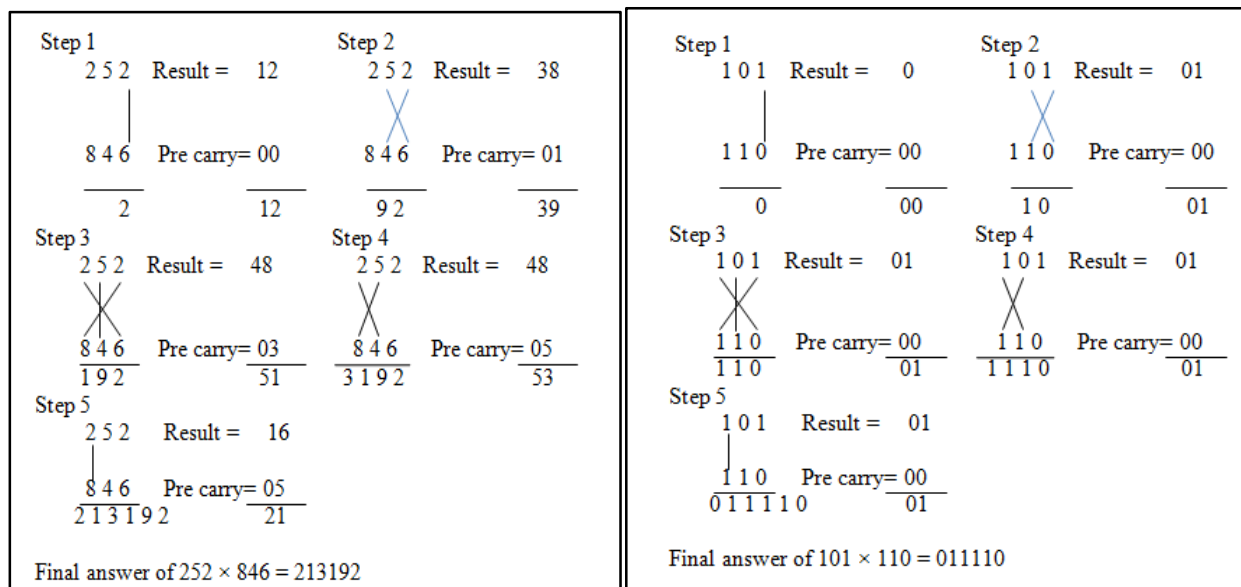
V. VEDIC MULTIPLIER

UrdhvaTiryakbhayam (UT) is a multiplier primarily based on Vedic mathematical algorithms formulated by ancient Indian Vedic mathematicians. The “UrdhvaTiryagbhayam” Sutra is a preferred multiplication formula relevant to all cases of multiplication along with binary, hex, decimal and octal. The Sanskrit word “Urdhva” means “Vertically” and “Tiryagbhayam” means “crosswise”. Fig 4 shows an example of UrdhvaTiryagbhayam. [3]

The partial products are generated parallel and simultaneous additions of the partial products are performed using this algorithm. Because of this the speed of the multiplier is improved significantly when compared to other procedures. [2]

The Algorithm: Multiplication of 101 by 110. [20]

1. We will take the right-hand digits and multiply them together. This will give us LSB digit of the solution.
2. Multiply LSB digit of the top number by the second bit of the bottom number and the LSB of the bottom number by the second bit of the top number. Once we have those values, add them together.
3. Multiply the LSB digit of bottom number with the MSB digit of the top one, LSB digit of top number with the MSB digit of bottom and then multiply the second bit of both, and then add them all together.
4. This step is similar to the second step, just move one place to the left. We will multiply the second digit of one number by the MSB of the other number.
5. Finally, simply multiply the LSB of both numbers together to get the final product.



Step 5

$$\begin{array}{r} 252 \\ \times 846 \\ \hline 213192 \\ 21 \end{array}$$

Result = 16
Pre carry= 05

(a) (b)
Fig. 4. UrdhvaTiryagbhayam algorithm (a) for decimal multiplication (b) binary multiplication

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 4, April 2016

VI. VEDIC MULTIPLIER USING REVERSIBLE LOGIC

The 2 X 2 UrdhvaTiryagbhyam multiplier using conventional logic will have 4 outputs. The logical expressions are given below. [18]

$$Q_0 = A_0.B_0$$

$$Q_1 = (A_1.B_0) \text{ xor } (A_0.B_1)$$

$$Q_2 = (A_0.A_1.B_0.B_1) \text{ xor } (A_1.B_1)$$

$$Q_3 = A_0.A_1.B_0.B_1$$

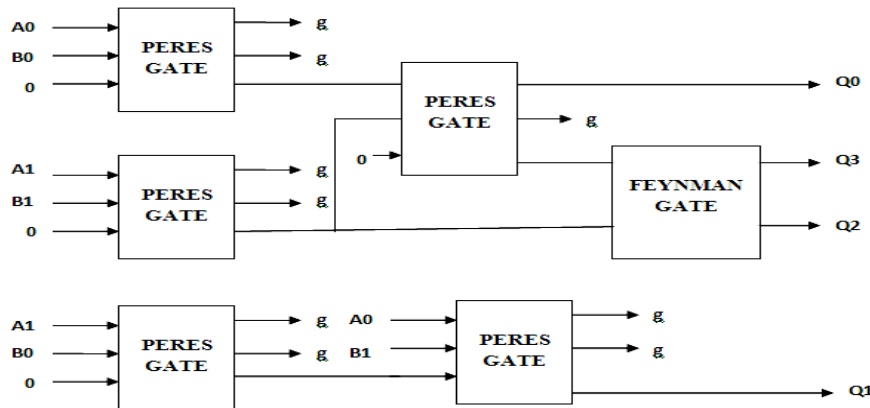


Fig. 5 A 2 X 2 UrdhvaTiryagbhyam Multiplier Unit

The reversible logic implementation of the above expressions has need of four peres gate and one Feynmen (CNOT) gate. The reversible logic implementation of 2 X 2 UT multiplier is shown in the Fig 5. The quantum cost of the 2X2 UrdhvaTiryakbhyam Multiplier is found to be 21. The number of garbage outputs is 9 and number of constant inputs is 4.

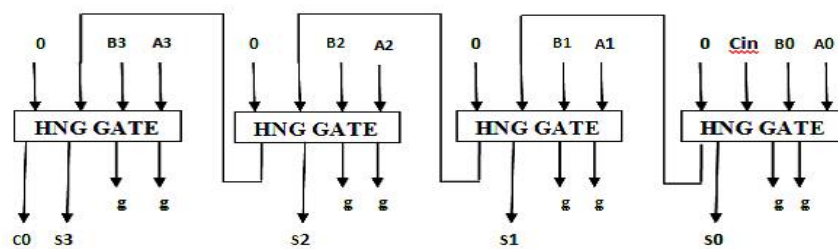


Fig. 6 Four bit ripple carry adder using HNG gate

The partial products generated using the 2 X 2 UT multiplier are need to be added using the four bit adder. The four bit ripple carry adder unit was designed using the HNG reversible gate. The four bit ripple carry adder unit using HNG gate is shown in the Fig 6.

The quantum cost of 4 bit adder unit using HNG gate is 24. The number of garbage output is 8 and constant input is 4. [20]

The architecture of 4 X 4 UrdhvaTiryagbhyam multiplier circuit is shown in the fig 7. It consist of four 2 X 2 UT multiplier unit and three 4 bit binary adders.

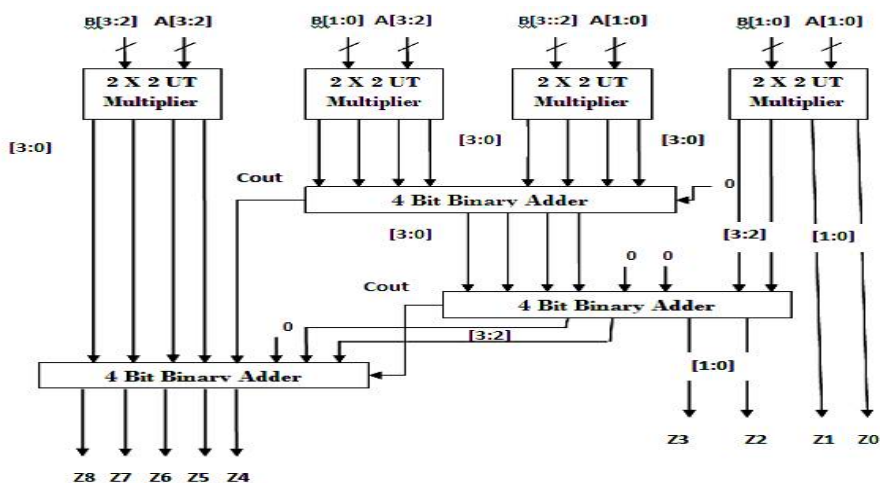


Fig. 7 A 4X4 UT multiplier using reversible logic gate

VII. CONCLUSION

In this paper the vedic multiplier using reversible logic method have been discussed. As per study the speed of a multiplier is increases by using UrdhvaTiryagbhyam multiplier and the negligible power can be achieved by reversible logic gate.

This paper presents the UrdhvaTiryakbhayam Vedic Multiplier realized using reversible logic gates. First 2X2 UT multiplier is designed using Peres gate and Feynmen gate. The ripple carry adders which were required for adding the partial products were constructed using HNG gates.

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